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## REMARKS

In the Office Action, the Examiner rejected claims 1-6, 8-11, 13, 16-18, 20-27, 29, and 32-46. By this paper, claim1 and 16 are amended. Claims 1-6, 8-11, 13, 16-18, 20-27, 29, and 32-46 remain pending in the present application and are believed to be in condition for allowance. In view the following remarks, Applicants respectfully request reconsideration and allowance of all pending claims.

*Claims 1-23 and 25-29*

The Examiner rejected claims 1-23 and 25-29 under 35 U.S.C. 103(a) as being anticipated by Leung et al (U.S. Patent No. 6,272,577, hereafter referred to as "the Leung reference") in view of Guttag (U.S. Patent No. 5,761,726, hereafter referred to as "the Guttag reference"). Applicants respectfully traverse the rejection.

***Legal Precedent***

First, the burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (PTO Bd. App. 1979). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). The mere fact that references *can* be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 16 U.S.P.Q.2d. 1430 (Fed. Cir. 1990). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill

in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985). The Examiner must provide *objective evidence*, rather than subjective belief and unknown authority, of the requisite motivation or suggestion to combine or modify the cited references. *In re Lee*, 61 U.S.P.Q.2d. 1430 (Fed. Cir. 2002).

***Independent Claim 1***

With respect to independent claim 1, the Examiner stated, in pertinent part:

> However, Leung does not specifically teach associating each of the plurality of target devices with a single base address, wherein the same single base address is associated with each of the plurality of target devices as recited in the claim.
>
> Guttag discloses associating each of the plurality of target devices with a single base address, wherein the same single base address is associated with each of the plurality of target devices [col. 172, lines 48-55] to generate addresses for read/write access to data stored within a plurality of memories (col. 5, ll. 40-45).

Office Action, pgs. 4 and 5.

Independent claim 1 recites, *inter alia,* "associating each of the plurality of target devices with *a single base address*, wherein *the same single base address is associated with each of the plurality of target devices*; sending a multicast transaction from the initiator device to the plurality of target devices, wherein sending the multicast transaction comprises sending a multicast transaction to *the single base address* associated with each of the plurality of target devices." (Emphasis added).

As admitted by the Examiner, the Leung reference fails to "teach associating each of the plurality of target devices with a single base address, wherein the same single base address is associated with each of the plurality of target devices as recited in the claim." Office Action, page 4. Furthermore, Applicants assert that the Guttag reference fails to obviate this deficiency of the Leung reference. Specifically, Guttag does not disclose associating each of the plurality of target devices with *a single base address*, wherein *the single base address is associated with each of the plurality of target devices*, as set forth in claim 1.

In making the rejection, it appears that the Examiner is looking at single phrase in the Guttag reference containing "base address" and taking it out of context. However, Applicants assert that when taken in context, it is clear that the Guttag reference does not disclose the features attributed to it by the Examiner. Claim 1 of the Guttag reference, a portion of which is referenced by the Examiner, is reproduced herein its entirety.

> A multi-processing system comprising:
> a plurality of m memories, each of said memories having *a unique addressable memory portion fixed upon manufacture within a single memory address space*;
> a plurality of n processors, where n is less than m and each of said n processors has a predetermined plurality of corresponding memories, said predetermined plurality of corresponding memories corresponding to each processor having a corresponding fixed base address *within said single memory address space*, each of said processors capable of generating any address within said single memory address space for read/write access to data stored within said single memory address space for read/write access to data stored within said plurality of m memories in accordance with received instructions, a base address instruction executing on any one of said plurality of n processors generating said base address of said predetermined plurality of memories corresponding to said one processor;

> a switch matrix connected to said plurality of m memories and said plurality of n processors responsive to an address generated by said processors to selectively *route data between a one of said plurality of n processors and a one of said plurality of m memories whose unique addressable memory portion encompasses said address.*

Guttag, col. 172, lines 43-67 (emphasis added).

As can be seen, the Guttag reference is directed to a multi-processing system with multiple memories where switches route requests from one of the processors to the appropriate memory. *See id.* Each processor is associated with a plurality of memories sharing the same base address within a single memory space. *Id.* Stated differently, each processor is associated with a base address which is shared by a plurality of memories. *See id.* As such, Guttag does not disclose associating each of the plurality of target devices with *a single base address*, wherein *the single base address* is associated with *each of the plurality of target devices*. Therefore, the Guttag reference does not obviate the deficiency of the Leung reference, with respect to claim 1.

Accordingly, the Leung reference and the Guttag reference, taken alone or in hypothetical combination, do not disclose all the features of independent claim 1. As such, Applicants respectfully request withdrawal of the Section 103 rejection and allowance of claim 1 and all claims depending therefrom.

***Independent claim 9***

In rejecting independent claim 9 the Examiner stated:

> Leung et al. discloses, a method for transacting data stored in memory between an initiator device and detecting a multicast transaction request [multiple bank operations such

> as broadcast-write and interleaved access possible; a memory device able to handle a broadcast write bandwidth of 36 gigabytes per second and 36 memory operations simultaneously; col. 5, lines 27-31]; accessing a first portion of memory by a first target device associated with the first portion of memory in response to the multicast transaction request[when a memory read or write command is decoded, each memory module is addressed, go into an idle state until the read or write transaction is finished; col. 19, lines 42-47]; accessing a second portion of memory by a second target device associated with the second portion of memory concurrently with access to the first portion of memory in response to the multicast transaction request wherein the first and second portions of memory are accessed with a single base address associated with the first target device and the second target device [a first field contains a base address which identifies the memory module by communication address. A second field contains an address which identifies the memory array within the memory module. col. 10, lines 21-25; the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus; col. 4, lines 20-24; in each memory module, a programmable identification register contains the base address of the memory module and a mechanism which decommissions the module from acting on certain memory access; col. 5, lines 5-8].

Office Action, pgs. 8 and 9.

Independent claim 9 recites, *inter alia*, "accessing a first portion of memory by a first target device in response to the multicast transaction request; and accessing a second portion of memory by a second target device concurrently with the access to the first portion of memory in response to the multicast transaction request, wherein the first and second portions of memory are accessed with *a single base address associated with both the first target device and the second target device.*" (Emphasis added).

As mentioned above with regard to claim 1, the Examiner admitted that the Leung reference fails to disclose "associating each of the plurality of target devices with a single

base address, wherein the same single base address is associated with each of the plurality of target devices." Applicants agree with the Examiner in this regard. However, in rejecting independent claim 9 the Examiner does not cite to any reference other than the Leung reference for the claim feature "wherein the first and second portions of memory are accessed with *a single base address associated with both the first target device and the second target device.*" Despite the Examiner's apparent failure to cite to the Guttag reference, Applicants address the rejection in view of the Guttag reference.

In sharp contrast to claim 9, the Leung reference clearly does not disclose the above mentioned features of claim 9. The cited portions of the Leung reference disclose a base address being associated with the memory module and another address associated with the memory array within the module. *See* Office Action, page 8; the Leung reference, col. 10, lines 21-25. The base address is used to address a *single module* and a second address to access a particular array within the single module. *See id.* Leung does not disclose, however, *first and second portions of memory* being accessed with *a single base address* associated with *both the first target device and the second target device*, as set forth in claim 9.

The Guttag reference fails to obviate the deficiencies of the Leung reference. Specifically, as discussed above, the Guttag reference discloses each processor being associated with a base address which is shared by a plurality of memories. *See* Guttag, col. 172, lines 43-67. However, Guttag does not disclose a *single base address* associated with both a first target device and a second target device. Accordingly, the Leung reference and the Guttag reference, taken alone or in hypothetical combination, do not disclose all the

features of independent claim 9. As such, Applicants respectfully request withdrawal of the rejection under Section 103 and allowance of claim 9, as well as all claims depending therefrom.

***Independent claim 16***

With respect to independent claim 16, the Examiner stated:

> [T]he rationale in the rejection of claim 1 is herein incorporated. Leung et al. further discloses, a computer system comprising a bus [memory device and allowing each memory module to have a communication address on the I/O bus system; col. 4, lines 54-56]; an initiator device coupled to the communications bus for initiation a transaction request [ all memory transactions are initiated by either I/O module 104 or by devices connected to I/O bus 106; col. 7, lines 45-46]; and a plurality of target devices coupled to the communications for executing the transaction request, the plurality of target devices executing the transaction request by each target device concurrently responding to a portion of the transaction request by each target device concurrently responding to a portion so the transaction request to the plurality of target devices using a single base address associated with the plurality of target devices [a first field contains a base address which identifies the memory module by communication address. A second field contains an address which identifies the memory array within the memory module. col.10, lines 21-25; a memory device in which a single input data stream can be simultaneously written to multiple memory arrays; col. 3, lines 63-65; a memory device in accordance with the present invention provides multiples commands, one after another , to different arrays; col. 25, lines 15-17; a base address which identifies the memory module; col. 10, lines 20-23; the memory modules are equipped with independent address and command decoders so that they function as independent units, each with their own base address; the present invention groups at least two memory arrays or banks into a memory modules and connects all the memory modules to a bus; col. 4, lines 20-24].

Office Action, pg. 10.

Independent claim 16 recites, *inter alia*, "a plurality of target devices coupled to the bus wherein each of the plurality of target devices concurrently executes a portion of the transaction request, wherein the initiator device is configured to multicast the transaction request to the plurality of target devices using *a single base address associated with the plurality of target devices, wherein the same single base address is associated with each of the plurality of target devices*." (Emphasis added).

The Leung reference does not disclose the above recited features of claim 16. Indeed, the Examiner admitted that the Leung reference fails to disclose "associating each of the plurality of target devices with a single base address, wherein the same single base address is associated with each of the plurality of target devices.". Similarly, the Leung reference does not disclose a single base address associated with each of the plurality of target devices, as set forth in claim 16. Additionally, the Guttag reference fails to obviate the deficiencies of the Leung reference in this regard. Specifically, the Guttag reference only discloses each processor being associated with a base address which is shared by a plurality of memories. *See* the Guttag reference, col. 172, lines 43-67. As such, the Leung reference and the Guttag reference, taken alone or in hypothetical combination do not disclose "*a single base address* associated with the *plurality of target devices*, wherein the *same single base address* is associated with *each of the plurality of target devices*," as set forth in independent claim 16. Accordingly, Applicants respectfully request withdrawal of Section 103 rejection and allowance of independent claim 16, as well as all claims depending therefrom.

***Independent Claim 25***

With respect to Independent claim 25, the Examiner stated:

> [T]he rationale in the rejection of claim 1 is herein incorporated. Leung et al. further discloses a computer system comprising a processor, a bus coupled to the processor [the two processors can reside on the same bus using the same memory module; col. 10, lines 40-42]; an initiator device coupled to the bus for issuing a multicast transaction, and a plurality of target devices coupled to the bus for executing the multicast transaction with concurrent data responses from a plurality of interleaved memory regions, wherein the initiator device is configured to multicast the transaction request to the plurality of target devices using a single base address associated with the plurality of target devices [all memory transactions are initiated by either I/O module 104 or by devices connected to I/O bus 106; col. 7, lines 45-46; multiple bank operations such as broadcast write and interleaved access possible. A memory device able to handle a broadcast write bandwidth of 36 gigabytes per second and 36 memory operations simultaneously; col. 5, lines 27-31; a first field contains a base address which identifies the memory module by communication address; col. 10, lines 21-25; the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus; col. 4, lines 20-24; in each memory module, a programmable identification register contains the base address of the memory module and a mechanism which decommissions the module from acting on certain memory access; col. 5, lines 5-8].

Office Action, pgs. 11 and 12.

Independent claim 25 recites, *inter alia,* "a plurality of target devices coupled to the bus, the plurality of target devices configured to execute the multicast transaction with concurrent data responses from a plurality of interleaved memory regions, wherein the initiator device is configured to multicast the transaction request to the plurality of target

devices using *a single base address associated with the plurality of target devices, wherein the same single base address is associated with each of the plurality of target devices.*"

In sharp contrast, the Leung reference does not disclose the above recited features of claim 25. Indeed, the Examiner admitted that the Leung reference fails to disclose "associating each of the plurality of target devices with a single base address, wherein the same single base address is associated with each of the plurality of target devices." Similarly, the Leung reference does not disclose a single base address associated with each of the plurality of target devices, as set forth in claim 25. Additionally, the Guttag reference fails to obviate the deficiencies of the Leung reference in this regard. Specifically, the Guttag reference only discloses each processor being associated with a base address which is shared by a plurality of memories. *See* the Guttag reference, col. 172, lines 43-67. As such, the Leung reference and the Guttag reference, taken alone or in hypothetical combination do not disclose "*a single base address* associated with the *plurality of target devices*, wherein the *same single base address* is associated with *each of the plurality of target devices,*" as set forth in independent claim 25. Accordingly, Applicants respectfully request withdrawal of Section 103 rejection and allowance of independent claim 25, as well as all claims depending therefrom.

***Independent claim 33***

Additionally, the Examiner rejected claims 33-38 under 35 U.S.C. § 103(a) as being unpatentable over the Leung reference in view of the Guttag reference and further in view of the Gupta reference (U.S. Pat. No. 6,405,286). Applicants respectfully traverse the rejection.

With respect to independent claim 33, the Examiner stated:

> [T]he rationale in the rejection of claim 1 is herein incorporated. However, Leung and Guttag do not specifically teach a method comprising dividing a section of memory into a plurality of interleaved memory regions as required by the claim.
>
> Gupta discloses a method comprising dividing a section of memory regions [col. 6, lines 20-24] so that multiple CPUs tend not to access the same memory bank at the same time (col. 6, ll 23-26).

Office Action pgs. 15-16.

Independent claim 33 recites, *inter alia*, "associating the plurality of target devices with a single base memory address, *wherein the same single base memory address is associated with each of the plurality of target devices*." (Emphasis added).

Applicants respectfully assert that several features of independent claim 33 are not disclosed by the Leung, Guttag and Gupta references, taken alone or in conjunction with each other. As described above with regard to claim 1, the Leung reference does not disclose the same single base address as recited in independent claims 33 and 36. Moreover, the Examiner admitted as much in the rejection of claim 1. Additionally, the Guttag reference does not obviate this deficiency of the Leung reference, as discussed in detail above. Furthermore, it is clear that the Gupta reference does not obviate this deficiency. The Gupta reference merely discloses a system which interleaves memory such that "multiple CPUs *tend not to access* the same memory bank at the same time," Gupta, col. 6, lines 22-25 (emphasis added). Indeed, the Gupta reference discloses a

plurality of memory buses that can simultaneously perform *independent memory transactions*, but where a single memory transaction can be active on *only one of those memory buses* at any given time. *See id.* at col. 16, lines 17-23. As such, the Gupta reference does not disclose that a single base memory address is associated with each of the plurality of target devices, as set forth in claim 33. Accordingly, the Leung, Guttag and Gupta references, taken alone or in hypothetical combination, do not disclose all the features of independent claim 33. As such, Applicants assert the Examiner has not established a *prima facie* case of obviousness with regard to independent claim 33. Therefore, Applicants respectfully request withdrawal of the rejection under Section 103 and allowance of claims 33 and 36, as well as all claims depending therefrom.

***Independent claim 36***

The Examiner rejected claim 36 under 35 U.S.C. § 103(a) as being unpatentable over the Leung reference in view of the Guttag reference and the Gupta reference. Specifically, the Examiner stated:

> As per claim 36 the rationale in the rejection of claim 1 is herein incorporated. Gupta further discloses a tangible machine readable medium comprising code to initialize a plurality of devices [col. 11, lines 36-39]; and code to associate the single base address with a plurality of interleaved memory regions [col. 6, lines 21-23]; col. 12, lines 44-55].

Office Action, pages 16-17.

Applicants respectfully traverse the rejection. Independent claim 36 recites, *inter alia*, "A tangible machine readable medium comprising...code to configure the plurality of devices to associate *a single base address* with the plurality of devices; and code to

associate the single base address with a plurality of interleaved memory regions, wherein *the same single base address* is associated with *each of the plurality of interleaved memory regions*." (Emphasis added).

As discussed above, the rejection of claim 1 is flawed. Specifically, the Leung reference and the Guttag reference, taken alone or in hypothetical combination do not disclose the *same single base address* being associated with each of the plurality of target devices. The Gupta reference fails to obviate the deficiencies of the Leung and Guttag references in this regard, as set forth above with respect to claim 33. As such, the Leung reference, the Guttag reference, and the Guttag reference, taken alone or in hypothetical combination, fail to disclose the same single base address being associated with each of the plurality of interleaved memory regions. Accordingly, Applicants respectfully request withdrawal of the rejection under Section 103 and allowance of independent claim 36, as well as all claims depending therefrom.

***Independent Claim 32***

The Examiner rejected claim 32 under 35 U.S.C. § 103(a) as being unpatentable over the Gupta reference in view of the Blaner reference. Specifically, the Examiner stated:

> Though Gupta discloses each of the devices simultaneously accesses interleaved memory region in response to a single transaction requests [two or more memory buses can each perform memory transactions simultaneously, with each memory bus coupled to one or more memory bus segments, wherein a single memory transaction can be active on a single memory bus segment at any give time, and each memory bus segment is coupled to one or more interleaved memory banks; col. 16, ll 15-23];

> Blaner also discloses each of the devices simultaneously accesses its associated interleaved memory region in response to a single transaction requests [interleaved memory banks wherein a group of the interleaved memory banks are accessible in parallel in response to a single access; col. 8, ll 22-26] to allow simultaneous access to multiple pages of memory and reduce latency (col. 2, ll 65-67).
>
> Office Action pg. 14.

Applicants respectfully traverse the rejection. Claim 32 recites, *inter alia*, "a plurality of devices, wherein each of the plurality of devices is associated with one of the interleaved memory regions and wherein each of the devices *simultaneously accesses* its associated interleaved memory region *in response to a single transaction request.*

Applicants respectfully assert that the Gupta reference fails to disclose all the elements of claim 32 and, further, that the Blaner reference fails to obviate the deficiencies of the Gupta reference. Specifically, with regard to the Gupta reference, contrary to the Examiner's assertions, the Gupta reference merely discloses a system which interleaves memory such that "multiple CPUs *tend not to access* the same memory bank at the same time," Gupta, col. 6, lines 22-25 (emphasis added). The Gupta reference explains that "the memory access patterns associated with multi-cached line interleaving will tend to be *independent and unrelated.*" *Id.* at lines 24-26. Indeed, the Gupta reference discloses a plurality of memory buses that can simultaneously perform *independent memory transactions*, but where a single memory transaction can be active on *only one of those memory buses* at any given time. *See id.* at col. 16, lines 17-23. As such, there is absolutely no mention in the Gupta reference of simultaneous accesses by each of the

plurality of devices "*in response to the single transaction request*," as recited in claim 32 (emphasis added). For at least this reason, Applicants respectfully assert that the Gupta reference does not disclose the above-recited features of claim 32.

The Blaner reference fails to obviate the deficiencies of the Gupta reference in this regard. Specifically, the Blaner reference discloses a first storage mechanism that can access a group of memory banks in parallel. Blaner, col. 8, lines 22-27. However, there is no mention in the Blaner reference of a plurality of devices, much less a plurality of devices where *each simultaneously accesses its associated interleaved memory region in response to a single transaction request*, as set forth in claim 32. As such, the Gupta reference and the Blaner reference, taken alone or in hypothetical combination, fail to disclose all the features of claim 32. Accordingly, Applicants respectfully request withdrawal of the Section 103 rejection and allowance of claim 32. Accordingly, Applicants respectfully request that the Examiner withdraw the Section 103 rejection based on the Gupta reference and the Blaner reference and allow independent claim 32.

***Claims 24 and 39-46***

Applicants respectfully assert that the Examiner has not established a *prima facie* case of obviousness with regard to dependent claims 24 and 39-46. The Examiner rejected claim 24 as obvious over the Leung reference in view of the Guttag reference and the Carmichael reference and rejected claims 39-46 as obvious over the Leung reference in view of the Guttag reference and the Olarig reference. However, as described above, the Leung and Guttag references clearly do not disclose those claim features attributed to it by the Examiner. In view of this deficiency, the Examiner's Section 103 rejections of claims

24 and 39-46, which are based upon the Examiner's mistaken interpretation of the Leung and Guttag references, cannot establish a *prima facie* case of obviousness. As such, Applicants respectfully request withdrawal of the Section 103 rejections of claims 24 and 39-46.

**Conclusion**

Applicants respectfully submit that all pending claims are in condition for allowance. However, if the Examiner wishes to resolve any other issues by way of a telephone conference, the Examiner is kindly invited to contact the undersigned attorney at the telephone number indicated below.

Respectfully submitted,

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